What is claimed is:

1. A failure detection system, comprising:

a wafer test information input unit configured to acquire pass/fail maps for respective wafers for a plurality of types of semiconductor devices, the pass/fail maps displaying failure chip areas based on results of a plurality of electrical tests performed on a plurality of chip areas assigned on the respective wafers;

an analogous test information input unit configured to classify the electrical tests into a plurality of analogous electrical tests with regard to analogous failures among the semiconductor devices;

a subarea setting unit configured to assign a plurality of subareas, each of which is common to the types of semiconductor devices on a surface of the wafer;

a characteristic quantity calculation unit configured to statistically calculate characteristic quantities based on a number of the failure chip areas included in the respective subareas for each of the analogous electrical tests; and

a categorization unit configured to obtain correlation coefficients between the characteristic quantities corresponding to the respective subareas of the wafers, and to classify clustering failure patterns of the failure chip areas into categories by comparing the correlation coefficients with a threshold value.

2. The system of claim 1, further comprising a product information input unit configured to append manufacturing records including manufacturing processes and manufacturing apparatuses for the semiconductor devices to the pass/fail maps.

3. The system of claim 1, wherein the characteristic quantities are failure densities of the failure chip areas displayed by the pass/fail maps for the respective subareas.

4. The system of claim 1, further comprising a failure category analysis unit configured to determine a cause of the failures by use of test statistics obtained by statistically analyzing deviations of records of manufacturing apparatuses based on manufacturing records of the wafers belonging to the categories.

5. The system of claim 4, wherein the test statistic is a chi-square test statistic.

6. The system of claim 4, further comprising a subarea database configured to store a plurality of area dividing methods of setting different subareas, each of the area dividing methods setting subareas common to the types of semiconductor devices.

7. The system of claim 6, further comprising a subarea optimization unit configured to determine an optimum area dividing method for the respective subareas set by the plurality of area dividing methods, by classifying the clustering failure patterns obtained from the pass/fail maps into the categories for each of the area dividing methods, obtaining the same category by determining analogies among the respective categories corresponding to each of the area dividing methods, and by comparing the test statistics calculated for the wafers belonging to the same category for each of the area dividing methods.

8. The system of claim 1, wherein the subareas are areas divided by combinations of at least one of concentric dividing circles concentric with a center of the wafer and a plurality of radial dividing lines drawn from the center with an equal angle having a length equal to a radius of the wafer.

9. The system of claim 1, wherein each of the subareas has an area including at least one of the chip areas.

10. A failure detection method, comprising:

manufacturing wafers having a plurality of types of semiconductor devices in manufacturing equipment;

acquiring pass/fail maps displaying failure chip areas based on results of a plurality of electrical tests performed

on a plurality of chip areas assigned on the respective wafers;

classifying the electrical tests into a plurality of analogous electrical tests with regard to analogous failures among the semiconductor devices;

assigning a plurality of subareas, each of which is common to the types of semiconductor devices on a surface of the wafer;

statistically calculating characteristic quantities based on a number of the failure chip areas included in the respective subareas for each of the analogous electrical tests; and

obtaining correlation coefficients between the characteristic quantities of the wafers corresponding to the subareas to classify clustering failure patterns of the failure chip areas into categories by comparing the correlation coefficients with a threshold value.

11. The method of claim 10, wherein the subareas are divided by combinations of at least one of concentric dividing circles concentric with a center of the wafer and a plurality of radial dividing lines drawn from the center with an equal angle having a length equal to a radius of the wafer.

12. The method of claim 10, wherein each of the subareas has an area including at least one of the chip areas.

13. The method of claim 10, wherein the characteristic quantities are failure densities of the failure chip areas displayed by the pass/fail maps for the respective subareas.

14. The method of claim 10, further comprising appending manufacturing records including manufacturing processes and manufacturing apparatuses of the semiconductor devices to the pass/fail maps.

15. The method of claim 10, further comprising determining a cause of the failures by use of test statistics obtained by statistically analyzing deviations of records of manufacturing apparatuses based on manufacturing records of the wafers belonging to the categories.

16. The method of claim 15, wherein different subareas common to the types of semiconductor devices are set as the subareas.

17. The method of claim 16, further comprising:

obtaining the same category by determining analogies among the respective categories corresponding to the respective different subareas;

determining the cause of the failures based on the subarea giving a maximum test statistic for the respective different subareas by comparing the test statistics

calculated for the different subareas for the wafers belonging to the same category when the wafers belonging to the same category are obtained among the different subareas.

18. The method of claim 15, wherein the test statistic is calculated from a chi-square test.

19. A computer program product configured to be executed by a computer, comprising:

an instruction of acquiring pass/fail maps for respective wafers of a plurality of types of semiconductor devices, the pass/fail maps displaying failure chip areas based on results of a plurality of electrical tests performed on a plurality of chip areas assigned on each of the respective wafers;

an instruction of classifying the electrical tests into a plurality of analogous electrical tests with regard to analogous failures among the semiconductor devices;

an instruction of assigning a plurality of subareas, each of which is common to the types of semiconductor devices on a surface of the wafer;

an instruction of statistically calculating characteristic quantities based on a number of the failure chip areas included in the respective subareas for each of the analogous electrical tests; and

an instruction of obtaining correlation coefficients

between the characteristic quantities of the wafers corresponding to the respective subareas to classify clustering failure patterns of the failure chip areas into categories by comparing the correlation coefficients with a threshold value.

20. The computer program product of claim 19, wherein the characteristic quantities are failure densities of the failure chip areas displayed by the pass/fail maps for the respective subareas.